## REMARKS/ARGUMENTS

Claims 1-11 are pending, and all pending claims are rejected. By this Amendment, independent claims 1 and 8 have been further amended. No claims are cancelled. Further consideration is requested in view of the above claim amendments and the following remarks.

Claims 1-4 and 8-11 stand rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,272,102 to Kahlman in view of U.S. Patent No. 3,310,751 to Atzenbeck. The rejection of these claims, as now amended, is respectfully traversed.

In the Final Office Action of July 14, 2011, the Examiner stated that:

> "Kahlman fails to explicitly disclose storing said detected minimum/maximum values only upon occurrence of a bit level change. However, in a similar field of endeavor, Atzenbeck discloses storing said detected minimum/maximum values only upon occurrence of a bit level change (col. 7, lines 20-31). Further, the storage of detected changed only upon level bit changes would have the advantage of saving power and processing by not continuously storing values. Therefore, for at least this reason, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the above-mentioned elements of Atzenbeck into the disclosure of Kahlman"

The Applicant respectfully traverses this characterization since it is deemed that Atzenbeck does not precisely detect a bit level change, but rather detects a hit (either positive hit 36 or negative hit 37) occurring in a data signal (signal 41 for instance). Because of the use of a cascade of three flip-flops 10-11-12 and the pattern detectors, Atzenbeck suppresses hits 37 and 38 shown below:

Fig.1.

"+" hit to suppress

"-" hit to suppress

Cleaned signal
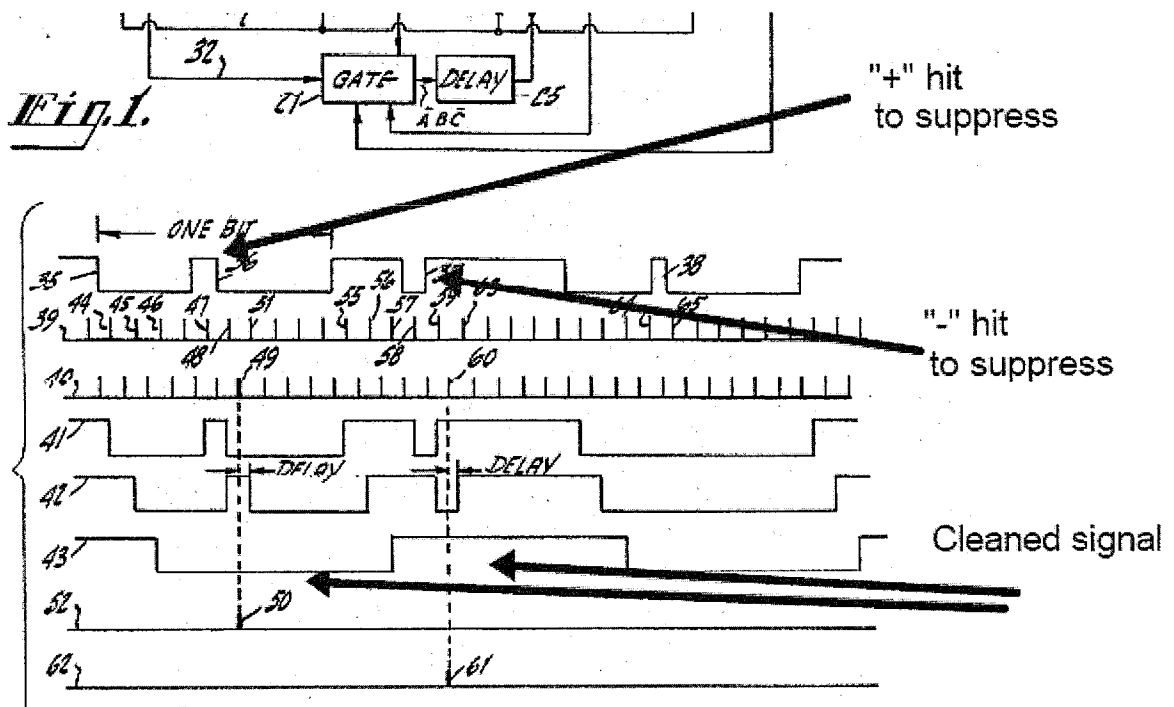
It should be noticed that such prior art is a subtle mechanism for filtering high frequencies peaks with only the use of digital techniques at a time where complex DSP resources and digital filters where not yet available.

See column 2, line 18:

> "A distortion detecting and correcting circuit for data signals is provided by the invention in the form of a filter using only digital techniques. The correction of the data signal is performed with a minimum of component parts and complexity, completely avoiding the filter design and other problems encountered in the analogue techniques previously employed to obtain a similar result."

Therefore, Atzenbeck has the same effect as using analog high pass filters, which would filter the data signal from the sharp hits 36, 37 etc.

However, in order to more clearly distinguish the present invention over the combination of Kahlman (U.S. Patent No. 6,272,102) and Atzenbeck (U.S. Patent No. 3,310,751), the Applicant has introduced additional limiting features in independent claims 1 and 8 as set forth above. Proper support for the amendments can be found in page 5, lines 11-32 of the published PCT application, and particularly line 21 below:

> "*To detect a rising slope, the slope detector compares the current maximum peak value, if there exists any at the output of detector 20, to the value of the previous minimum peak stored in the buffer 34. A rising slope is detected only if the current maximum peak value is higher than the previous minimum peak value plus a predetermined threshold.*
>
> *To detect a falling slope, the slope detector compares the current minimum peak value, if there exists any at the output of detector 22, to the value of the previous maximum peak stored in buffer 32. A falling slope is detected only if the previous maximum peak value is higher than the current minimum peak value plus a predetermined threshold.*"

It is deemed that, because of the new claimed limitations, the subject matter of the newly amended independent claims 1 and 8 will be considered as being allowable since it is clear that, in Atzenbeck, there is no equivalent means for computing the difference between two successively detected maximum values. These limitations are not deemed to be suggested by Kahlman, nor in the combination of references.

Due to the distinguishing features now claimed in claims 1 and 8, a significant advantage is achieved that in a noisy signal or also in long sequences of "0" or "1" (such as shown in bit period n°2 or bit period n°9 or still bit period n°11) there is no storage of any new MAX or MIN values, thus providing a stronger slicer threshold as explained in page 9 of the originally filed application:

> *"It should be noted that during one bit period n°2, no rising slope is detected since the value of peak 3 is equal to the value of the previous minimum peak (peak 0).*
> *During one bit period n°9 and during one bit period n°1 1 neither shift register 24 nor shift register 26 is activated since this corresponds to a long logic "1" sequence and a long logic "0" sequence, respectively. Therefore, even if the amplitude of the binary signal corresponding to a long logical "1" or "0" sequence varies due to noise, for example, only one maximum or minimum peak value is stored. Consequently, the generated slicer threshold is not sensitive to long logical "1" or "0" sequences in the binary signal."*

For the above reasons, claims 1 and 8 are deemed to be patentable and allowable over the combination of the cited references. The remaining dependent claims are deemed to be allowable as being dependent upon either allowable base claim 1 or base claim 8.

Claims 5-7 stand rejected under 35 USC 103(a) as being unpatentable over Kahlman and Atzenbeck, and further in view of Lavrenov, GB 1,566,1609. This rejection is also respectfully traversed. Claims 5-7 are deemed to be allowable as being dependent upon allowable base claim 1 for the reasons stated above.

In view of all of the above, the claims are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicant's attorney at the telephone number listed below.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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